Additionally, the Examiner rejected claims 1, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 20, 21, 25, and 26 under 35 U.S.C. § 102(b) as anticipated by Masayuki (U.S. Patent No. 6,262,488); rejected claims 2, 3, 6, 8, 16, and 18 under 35 U.S.C. § 103(a) as unpatentable over Masayuki in view of Kasa (U.S. Patent No. 5,179,536); and rejected claims 22 and 23 under 35 U.S.C. § 103(a) as unpatentable over Masayuki in view of Chen (U.S. Patent No. 5,761,609).

I. REJECTION OF CLAIMS 1, 5, 7, 9-15, 17, 19-21, AND 25-26 UNDER §102(b)

Applicant respectfully traverses the Examiner's rejection of claims 1, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 20, 21, 25, and 26 under 35 U.S.C. § 102(b) as anticipated by Masayuki for the following reasons.

To anticipate claim 1 under 35 U.S.C. § 102(b), Masayuki, taken individually, must explicitly disclose each and every element recited in the claim either expressly or inherently. *See* M.P.E.P. § 2131. However, Masayuki does not teach each and every element recited in claim 1. Applicant's claim 1 patentably distinguishes the present invention from the teachings of Masayuki. Thus, Masayuki does not anticipate claim 1.

Masayuki discloses a semiconductor device with a module base plate 1, which is "constructed by stacking pluralities of ceramic layers and wiring layers by the use of laminated ceramic." *See* col. 5, lines 37-40. This is accomplished by stacking eight semiconductor chips on each of the front surface and rear surface of the module base plate 1. *See* col. 5, lines 40-42. Each semiconductor chip includes a static RAM and bump electrodes 6 to which various leads 5A, 5B, 5C, and 5D are respectively connected. *See* col. 5, lines 47-50. The individual leads 5B are connected to a

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decoder 3 and leads 2 through wiring. *See* col. 5, lines 64-66. Finally, the lead 5A, for inputting a chip select signal to the semiconductor chip 4A is connected to the lead 3A of the decoder 3 without being connected with the lead 5B for inputting a chip select signal to the semiconductor chip 4B. *See* col. 5, line 66 to col. 6, line 3. Accordingly, Masayuki is directed to a technique for stacking memory chips.

Claim 1 includes, among other things, "an identifying unit which includes at least a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal, and an identifier generating circuit for generating identifiers for other memory units on the basis of the identifier." At the very least, Masayuki does not disclose these exemplary features.

Furthermore, the Examiner merely alleges the following, as a basis for rejecting claim 1: "Regarding claim 1, in Fig. 1 and Fig. 18, Masayuki et al. [shows] a semiconductor device with memory units labeled as 4A in Fig. 1 and RAM in Fig. 18, selecting terminals WE, OE, A, DS, CS and I in Fig. 18, and a decoder that functions as [an] identifier [that is] labeled decoder in Fig. 18 and 3 in Fig. 1" (Office Action, page 2). Applicant respectfully deems this rejection insufficient for the following reasons.

First, Applicant respectfully submits that the Examiner has not addressed Applicant's previously made arguments in the response filed September 23, 2002. In view of the unresponsive nature of the Examiner's response, Applicant respectfully draws the Examiner's attention to M.P.E.P. § 707.07 and 37 C.F.R. § 1.104(b), which mandate that an Examiner's Office Action be complete as to all matters. In that regard, the Examiner's response does not address Applicant's previously filed arguments.

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Accordingly, Applicant deems the finality of the present Office Action to be premature and specifically requests that it be withdrawn.

Second, the Examiner's rejection of claim 1 does not account for all of the features of the present invention as claimed. As mentioned earlier, to anticipate claim 1 under 35 U.S.C. § 102(b), Masayuki, taken individually, must explicitly disclose each and every element recited in the claim either expressly or inherently. *See* M.P.E.P. § 2131. In the Office Action, the Examiner fails to provide any citation to, or support found within, Masayuki that expressly or inherently discloses at least "an identifying unit . . . for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal," as recited in independent claim 1. At the very least, Masayuki does not teach this feature. Moreover, the Examiner fails to account for this feature in the rejection of claim 1. Simply alleging that Masayuki includes "a decoder that functions as [an] identifier [that is] labeled decoder" does not mention, nor account for, "an identifying unit . . . for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal," as recited in claim 1. For at least these reasons, the Examiner should withdraw the rejection of claim 1 and withdraw the finality of the last Office Action.

Independent claim 10 includes, among other things, "an identifying unit which is provided outside the memory unit and includes at least a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned thereto and a memory unit selecting signal." In the Examiner's rejection of claim 10, the Examiner only states "there are multiple of memories" (Office Action, page 3). Moreover, the Examiner does not point to a prior art reference that discloses all of the features of

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independent claim 10. Applicant respectfully deems this rejection insufficient because it does not account for each and every element of claim 10. For at least these reasons, the Examiner should withdraw the rejection of claim 10 and withdraw the finality of the last Office Action.

Next, independent claim 15, includes, among other things, "a first identifying unit including at least: a first memory unit selecting circuit for selecting the first memory unit on the basis of a first identifier assigned thereto and the memory unit selection signal." The Examiner merely alleges Masayuki discloses "there are two decoders and multiple of select signals" (Office Action, page 3). Again, Applicant respectfully deems this rejection insufficient because it does not account for each and every element of claim 15. For at least these reasons, the Examiner should withdraw the rejection of claim 15 and withdraw the finality of the last Office Action.

Finally, independent claim 25 includes, among other things, "an identifying unit at least including an identifier generating circuit provided with at least a wire for generating an identifier for the memory unit, and a memory unit selecting circuit for selecting the memory unit on the basis of the identifier assigned thereto and the memory unit selecting signal." For this claim, the Examiner only alleges "decoder and select signals are connected with a wire" (Office Action, page 3). Again, Applicant respectfully deems this rejection insufficient because it does not account for each and every element of claim 25. For at least these reasons, the Examiner should withdraw the rejection of claim 25 and withdraw the finality of the last Office Action.

In sum, Masayuki fails to disclose all of the features of independent claims 10, 15, and 25. Accordingly, Masayuki cannot anticipate these claims because Masayuki,

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taken individually, fails to explicitly disclose each and every element recited in these claim either expressly or inherently as required under § 102(b). The Examiner should thus withdraw the rejection of claims 10, 15, and 25.

Claims 3-5, 7, 9-14, 17, 19-21, and 26, which each depend from one of independent claims 1, 10, 15, and 25, respectively, recite additional features that are neither disclosed expressly or inherently by Masayuki. Claims 3-5, 7, 9-14, 17, 19-21, and 26, are thus allowable at least due to their dependence upon allowable independent claims 1, 10, 15, and 25.

II. REJECTION OF CLAIMS 2, 3, 6, 8, 16, AND 18 UNDER § 103(a)

Because the Examiner has not established a *prima facie* case of obviousness, Applicant respectfully traverses the rejection of claims 2, 3, 6, 8, 16, and 18 under 35 U.S.C. § 103(a).

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, the Examiner must demonstrate each of the following three requirements. First, Masayuki and Kasa, when combined as a whole, must disclose or suggest each and every element recited in the claims. *See* M.P.E.P. § 2143.03. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. *See id.* Third, a reasonable probability of success must exist. *See id.* Furthermore, each of these requirements must be found in the prior art, and not based on applicant's disclosure. *See* M.P.E.P. § 2143.

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Kasa is directed to a semiconductor memory device comprising memory cells for pre-storing fixed data and for replacing defective memory cells. For example, Kasa states that the "defective memory cell within the mask ROM cell array 16 is substituted by the PROM cell array 23 and the defective memory cells are relieved." *See* col. 5, lines 41-44. As discussed above, Masayuki does not disclose each and every element recited in independent claims 1 and 15. Furthermore, Kasa fails to make up for the deficiencies of Masayuki. Accordingly, neither Masayuki nor Kasa taken alone or in any reasonable combination teaches or suggests at least the above elements of independent claims 1 and 15.

Claims 2, 3, 6, 8, 16, and 18 each depend from independent claims 1 and 15. For at least this reason, the combination of Masayuki and Kasa fails to disclose or suggest each and every element recited in claims 2, 3, 6, 8, 16, and 18.

Furthermore, Applicant respectfully submits that the Examiner has not shown that the combination of Masayuki and Kasa would provide the artisan or one of ordinary skill with a suggestion or motivation, at the time of making the invention, to combine the references so that it would include all of the elements recited in claims 2, 3, 6, 8, 16, and 18.

A statement by the Examiner that "[i]t would have been obvious to one of having ordinary skill in the art to include an adder circuitry, a comparator in decoder and associated circuitry in an programmable memory [of] Masayuki et al. as taught by Kasa et al. because such structure would provide a better flexibility" does not meet the burden of showing the necessary motivation to make the proposed combination and is insufficient to support the rejection (Office Action, page 4). Kasa is directed to a

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semiconductor memory device comprising memory cells for pre-storing fixed data and for replacing defective memory cells. No motivation exists for combing the teachings of Kasa with the stacking method for semiconductor chips disclosed in Masayuki. In the absence of a factual basis that would demonstrate the suggestion or motivation to combine the references in a manner resulting in the claimed invention, a *prima facie* case of obviousness has not been made and the Examiner should withdraw the rejection.

Finally, the Examiner has also failed to demonstrate a reasonable probability of success of modifying Masayuki with the teachings of Kasa.

For at least the above reasons, Masayuki and Kasa fail to suggest or motivate each and every element recited in claims 2, 3, 6, 8, 16, and 18. Moreover, claims 2, 3, 6, 8, 16, and 18, which each depends upon one of the independent claims, respectively, recite additional features that are neither disclosed nor suggested by any of the cited references, taken either alone or in any reasonable combination. Accordingly, claims 2, 3, 6, 8, 16, and 18 are allowable for at least the same reasons discussed above with respect to allowable independent claims 1 and 15. For at least these reasons, Applicant respectfully requests the Examiner to withdraw the rejection and allow claims 2, 3, 6, 8, 16, and 18.

III. REJECTION OF CLAIMS 22 AND 23 UNDER § 103(a)

Applicant respectfully traverses the rejection of claims 22 and 23 under 35 U.S.C. § 103(a) as unpatentable over Masayuki in view of Chen for the following reasons.

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Chen discloses a limited use circuit that may be used only a limited number of times so that copying or unauthorized use of an electronic system may be prevented. *See* col. 2, lines 36-40. In contrast, independent claim 22 includes, among other things, "an identifying unit at least including an identifier generating circuit provided with at least a fuse element for generating an identifier assigned to the memory unit." Neither Masayuki nor Chen taken alone or in any reasonable combination teaches or suggests at least these elements. As claim 23 depends from independent claim 22, for at least this reason the combination of Masayuki and Chen fails to disclose or suggest each and every element recited in claims 22 and 23.

Additionally, the Examiner states that "it would have been obvious to one of having ordinary skill in the art to include a fuse and resistor structure to the semiconductor module of Masayuki et al. as taught by Chen because such structure would provide a better programmability" (Office Action, page 4). Chen discloses a limited use circuit that may be used only a limited number of times. Nothing in Chen motivates or discloses a combination including "an identifying unit at least including an identifier generating circuit provided with at least a fuse element for generating an identifier assigned to the memory unit," as recited in claim 22. The Examiner's allegation without any factual evidence, such as a citation to a competent reference, does not meet the burden of showing the necessary motivation to make the proposed combination and is insufficient to support the rejection.

For at least these reasons, Masayuki and Chen fail to motivate or suggest each and every element recited in claims 22 and 23. Moreover, claims 22 and 23 recite additional features that are neither disclosed nor suggested by any of the cited

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